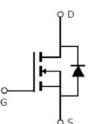


### **Main Product Characteristics:**

V <sub>DSS</sub>	75V
R <sub>DS</sub> (on)	6.5mohm(typ.)
$I_D$	80A







D2PAK

Marking and pin
Assignment

Schematic diagram

#### **Features and Benefits:**

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature



### **Description:**

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

# **Absolute max Rating:**

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ TC = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V①	80	
I <sub>D</sub> @ TC = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V①	70	Α
I <sub>DM</sub>	Pulsed Drain Current②	320	
D @TC = 25°C	Power Dissipation③	187	W
P <sub>D</sub> @TC = 25°C	Linear Derating Factor	2.0	W/°C
V <sub>DS</sub>	Drain-Source Voltage	75	V
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy @ L=0.3mH②	375	mJ
I <sub>AR</sub>	Avalanche Current @ L=0.3mH2	50	А
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C



### **Thermal Resistance**

Symbol	Characterizes	Тур.	Max.	Units
$R_{ heta JC}$	Junction-to-case③	_	0.8	°C/W
В	Junction-to-ambient (t $\leq 10s$ ) $\oplus$	_	62	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mounted, steady-state) ④	_	40	°C/W

## **Electrical Characterizes** $@T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions	
V <sub>(BR)DSS</sub>	Drain-to-Source breakdown voltage	75	_	_	V	V <sub>GS</sub> = 0V, ID = 250μA	
Б	Static Prair to Course on registance	_	6.5	8	0	V <sub>GS</sub> =10V,I <sub>D</sub> = 30A	
$R_{DS(on)}$	Static Drain-to-Source on-resistance	_	12.5	13	mΩ	T <sub>J</sub> = 125°C	
\/	Cata threshold voltage	2	_	4	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
$V_{GS(th)}$	Gate threshold voltage	_	2.35	_	V	T <sub>J</sub> = 125°C	
	Durin to Course leakens aument	_	_	1		$V_{DS} = 75V, V_{GS} = 0V$	
I <sub>DSS</sub>	Drain-to-Source leakage current	_	_	50	μA	T <sub>J</sub> = 125°C	
	Cata to Source forward lookage	_	_	100	nΛ	V <sub>GS</sub> =20V	
I <sub>GSS</sub>	Gate-to-Source forward leakage	-100	_	-	nA	V <sub>GS</sub> = -20V	
Qg	Total gate charge	_	93.6	_		I <sub>D</sub> = 30A,	
Q <sub>gs</sub>	Gate-to-Source charge	_	20.2	_	nC	V <sub>DS</sub> =30V,	
Q <sub>gd</sub>	Gate-to-Drain("Miller") charge	_	33.3	_		V <sub>GS</sub> = 10V	
t <sub>d(on)</sub>	Turn-on delay time	_	17.3	_			
tr	Rise time	_	15.2	-		V <sub>GS</sub> =10V, VDS=30V,	
t <sub>d(off)</sub>	Turn-Off delay time	_	52	-	ns	$R_L=15\Omega$ ,	
t <sub>f</sub>	Fall time	_	19	-		$R_{GEN}$ =2.5 $\Omega$	
C <sub>iss</sub>	Input capacitance	_	4373	_		V <sub>GS</sub> = 0V	
Coss	Output capacitance	_	352	_	pF	V <sub>DS</sub> = 25V	
C <sub>rss</sub>	Reverse transfer capacitance	_	306	_		f = 1MHz	

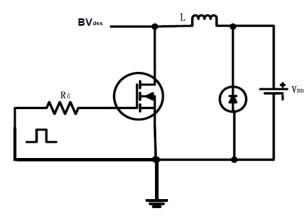
# **Source-Drain Ratings and Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current		-	80	А	MOSFET symb
	(Body Diode)	_				showing the
I <sub>SM</sub>	Pulsed Source Current		_	320	Α	integral reverse
	(Body Diode)	_				p-n junction diode.
V <sub>SD</sub>	Diode Forward Voltage	_	0.85	1.3	V	I <sub>S</sub> =30A, V <sub>GS</sub> =0V
t <sub>rr</sub>	Reverse Recovery Time	_	36	_	ns	$T_J = 25^{\circ}C$ , $I_F = 75A$ , $di/dt =$
Q <sub>rr</sub>	Reverse Recovery Charge	_	62	_	nC	100A/μs

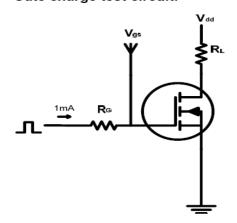


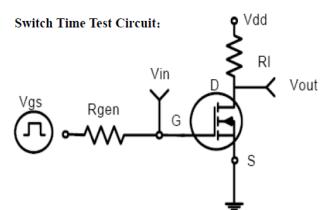
### **Test circuits and Waveforms**

#### EAS test circuits:

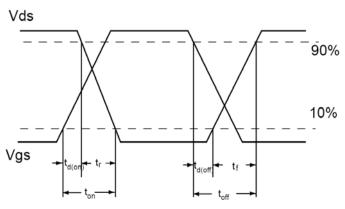


#### Gate charge test circuit:





#### **Switch Waveforms:**

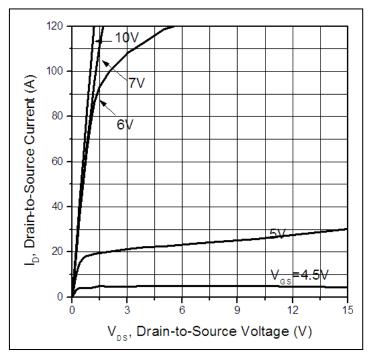


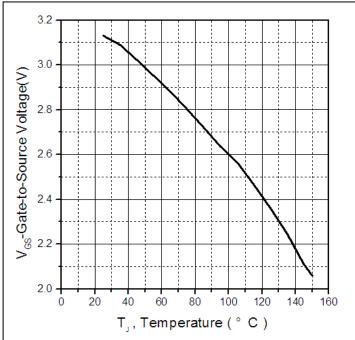
#### Notes:

- ①The maximum current rating is limited by bond-wires.
- ②Repetitive rating; pulse width limited by max. junction temperature.
- ③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- 4 The value of  $R_{\theta JA}$  is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C
- ⑤These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175$ °C.
- ⑥ The maximum current rating is limited by bond-wires.



# Typical electrical and thermal characteristics





**Figure 1: Typical Output Characteristics** 

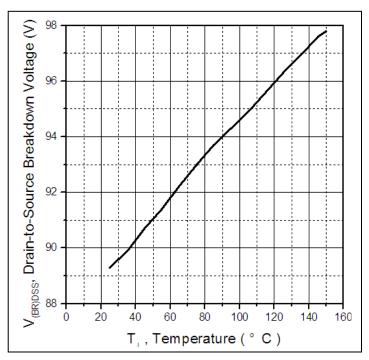


Figure 3. Drain-to-Source Breakdown Voltage vs.
Temperature

Figure 2. Gate to source cut-off voltage

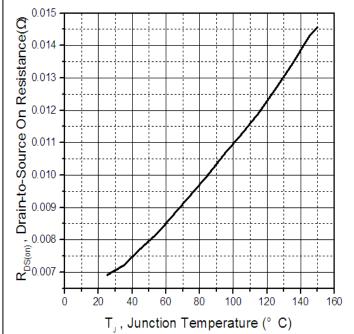
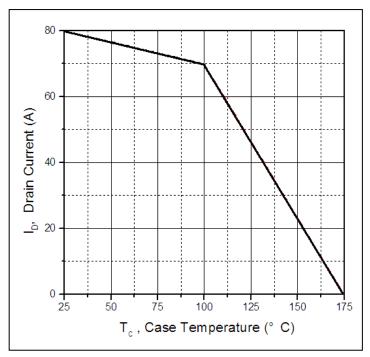


Figure 4: Normalized On-Resistance Vs. Case Temperature



## Typical electrical and thermal characteristics



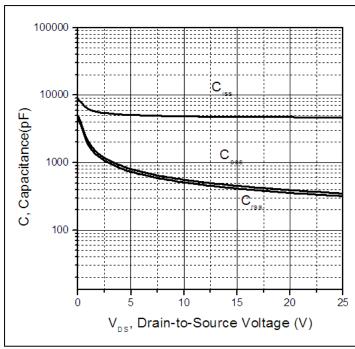


Figure 5. Maximum Drain Current Vs. Case Temperature

Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

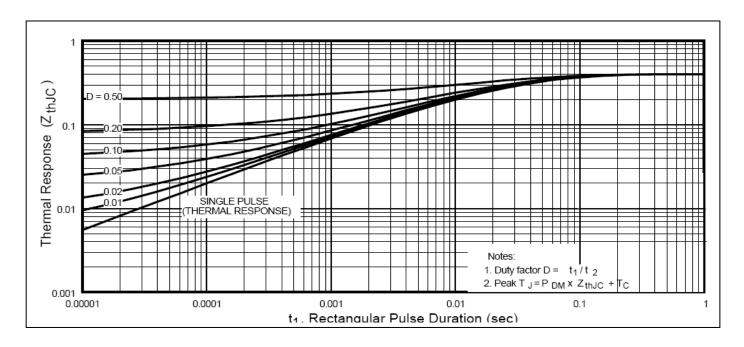
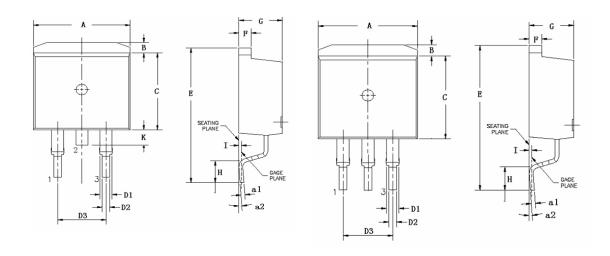


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case



# **Mechanical Data:**

### **TO263 PACKAGE OUTLINE DIMENSION**



Cumb ol	Dimension I	n Millimeters	Dimension In Inches		
Symbol	Min	Max	Min	Max	
Α	9.660	10.280	0.380	0.405	
В	1.020	1.320	0.040	0.052	
С	8.590	9.400	0.338	0.370	
D1	1.140	1.400	0.045	0.055	
D2	0.700	0.950	0.028	0.037	
D3	5.080	(TYP)	0.200 (TYP)		
E	15.090	15.390	0.594	0.606	
F	1.150	1.400	0.045	0.055	
G	4.300	4.700	0.169	0.185	
Н	2.290	2.790	0.090	0.110	
I	0.250 (TYP)		0.010	(TYP)	
K	1.300	1.600	0.051	0.063	
a1	0.450	0.650	0.018	0.026	
a2	00	8 <sup>0</sup>	1 <sup>0</sup>	8 <sup>0</sup>	



## **Ordering and Marking Information**

Device Marking: SSF7509A

Package (Available)
D2PAK
Operating Temperature Range
C: -55 to 175 °C

## **Devices per Unit**

Packag e Type	Units/Tu be	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
				DOX	
D2PAK	50	20	1000	6	6000

**Reliability Test Program** 

Test Item	Conditions	Duration	Sample Size
High	T <sub>j</sub> =125℃ to 175℃ @	168 hours	3 lots x 77 devices
Temperature	80% of Max	500 hours	
Reverse	V <sub>DSS</sub> /V <sub>CES</sub> /VR	1000 hours	
Bias(HTRB)			
High	T <sub>j</sub> =150℃ or 175℃ @	168 hours	3 lots x 77 devices
Temperature	100% of Max V <sub>GSS</sub>	500 hours	
Gate		1000 hours	
Bias(HTGB)			



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